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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,761	02/08/2001	Shigeru Onoya	12732-013001/ US4610	4159

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,761	ONOYA, SHIGERU	
	Examiner	Art Unit	
	Alexander Eisen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-15 and 18-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15 and 18-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01 February 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 and 6-9, 11, 14, 18, 19, 21, 22, 27 and 40-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirakata, US 6,496,172 B1.

With respect to claim 1 Hirakata discloses a method for driving a semiconductor display device wherein display signals input to pixel electrodes in a vertical line have a same polarity and the same polarity is independently controlled for each vertical line of the plurality of pixels, and wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period (FIG. 1A; col. 9, lines 34-67).

In regard to claim 2 Hirakata additionally discloses that the method wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces the flicker (see abstract; col. 5, lines 40-45).

As to claim 3, Hirakata further discloses that the method of driving a semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces vertical striping (col. 10, lines 40-46).

As to claim 6, Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods (compare frame periods 1-4 in FIG. 1A, fore example).

As to claim 7, Hirakata also discloses a semiconductor display device comprising a source signal line driver circuit 105 (FIG. 2); a gate signal driver circuit (104); a plurality of source signal lines 103; a plurality of gate signal lines 102; a pixel portion (display region 106); a display signal generation portion which has a control portion 108, a polarity data signal generation portion 208; a display signal selection portion 109, a + side display signal generation portion 201; a - side display signal generation portion, and wherein display signals input to display electrodes in a vertical line have the same polarity, and the same polarity is independently controlled for each vertical line of the plurality of pixels, and wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period.

As to claim 8, Hirakata additionally discloses that the method wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces the flicker.

As to claim 9, Hirakata further discloses that the method of driving a semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces vertical striping, and wherein the same polarity is independently controlled for each vertical line of the plurality of pixels.

As to claim 11, Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods.

As to claim 14 Hirakata further teaches that the semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period have reduced vertical striping, and polarities of the display signals input to pixel electrodes in a vertical lines change together.

As to claims 18-19, 21-22 and 27 Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods.

Regarding claims 40 and 44, while Hirakata discloses at least four kinds of polarity patterns, where the polarity of signals inputted to a vertical line is the same, the patterns being sequentially displayed in one period of frames, the number of which (frames) is the same as of that of the kinds of polarity patterns (col. 6, ll. 18-33), Hirakata also teaches that the number of vertical lines inverted at the same time can be three or more (4), and then the number of different polarity patterns (and therefore the number of frames in the sequence period) can be equal Z=3!=6 or Z=4!=24 respectively, meaning that the interval within which the patterns will be repeated will be equal to 6 or 24 consecutive frames, i.e. well within the requirements of claims 40 and 44, more than four frame period (col. 14; ll. 41-67).

Claims 41-43 and 45-57 recite the limitations similar to that of claims 2 and 6, and therefore are rejected on the same grounds.

4. Claims 4, 10, 12, 13, 15, 20, 23-26, and 28-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Cole, US 6,469,684 B1.

With respect to claim 4 Cole discloses a method of driving a semiconductor display device comprising a plurality of pixels 32 (FIG. 4A) each containing a pixel TFT 52 and pixel electrode 54; and a liquid crystal formed between the pixel electrode and opposing electrode (col. 7, lines 46-50); wherein display signals are input to the pixel electrode through the pixel TFT, wherein each of the display signal has one of a positive and negative polarity, wherein the pixel electrodes are arranged in multiple vertical lines and polarities of the display signals input to pixel electrodes in a vertical lines change together; and wherein pixels to which display signals having a particular polarity are input change randomly in a certain fixed period (frame; see Fig. 3; col. 5, lines 47-59).

As to claim 10, Cole discloses a semiconductor display device comprising a source signal line driver circuit 102 (FIG. 5); a gate signal driver circuit (104); a plurality of source signal lines 116; a plurality of gate signal lines 118; a pixel portion (display region 120); a display signal generation portion which has a control portion, a polarity data signal generation portion 152; an alternating current generation portion 156; a display signal selection portion, a + side display signal generation portion 142; a - side display signal generation portion 144, and wherein display signals input to display electrodes in a vertical line have the same polarity, and polarities of the display signals input to pixel electrodes in a vertical lines change together, and wherein pixels to

which display signals having a particular polarity are input are changed randomly in a certain fixed period.

As to claim 12 Cole further discloses a method of driving a semiconductor display device comprising a plurality of pixels 32 (FIG. 4A) each containing a pixel TFT 52 and pixel electrode 54; and a liquid crystal formed between the pixel electrode and opposing electrode (col. 7, lines 46-50); wherein display signals are input to the pixel electrode through the pixel TFT, wherein each of the display signal has one of a positive and negative polarity, and polarities of the display signals input to pixel electrodes in a vertical lines change together; and wherein pixels to which display signals having a particular polarity are input change randomly in a certain fixed period so that the flicker become difficult to observe (col. 9, lines 39-47).

As to claim 13 Cole discloses a semiconductor display device comprising a source signal line driver circuit 102 (FIG. 5); a gate signal driver circuit (104); a plurality of source signal lines 116; a plurality of gate signal lines 118; a pixel portion (display region 120); a display signal generation portion which has a control portion, a polarity data signal generation portion 152; an alternating current generation portion 156; a display signal selection portion, a + side display signal generation portion 142; a - side display signal generation portion 144, and polarities of the display signals input to pixel electrodes in a vertical lines change together, and wherein pixels to which display signals having a particular polarity are input are changed randomly in a certain fixed period so that the flicker become difficult to observe.

As to claims 15, 20 and 23 as can be seen from Fig. 3 a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods (compare column 2 in frames 2 and 3 for example).

As to claim 24 Cole discloses a method of driving a semiconductor display device comprising a plurality of pixels 32 (FIG. 4A) each containing a pixel TFT 52 and pixel electrode 54; an opposing electrode and a liquid crystal formed between the pixel electrode and opposing electrode (col. 7, lines 46-50); wherein display signals are input to the pixel electrode through the pixel TFT, wherein each of the display signal has one of a positive and negative polarity and polarities of the display signals input to pixel electrodes in a vertical lines change together; and wherein pixels to which display signals having a particular polarity are input change randomly in a certain fixed period so that the vertical striping become difficult to observe due to random switching of pixel polarities.

As to claims 25 and 26 as can be seen from Fig. 3 a polarity of display signals input to only some of the pixel electrodes have an inverse polarity in two adjacent frame periods.

As to claims 28-37, as can be seen from FIG. 3 the polarity of the pixel signals inputted to all of the pixels in vertical line is changed randomly in certain fixed period and the polarity of the display signals inputted to multiple ones of the vertical lines of pixel electrodes are changed randomly in certain fixed period (see frame two in FIG. 3, wherein the polarity of two vertical lines, 1 and 2 are of the same polarity for all the pixels in the vertical line and wherein the polarity is changed randomly in consecutive frames, frame 3 - frame 4 - frame 1 in certain fixed period of time).

Response to Arguments

5. Applicant's arguments with respect to claims 1-4 and 6 have been fully considered but they are not persuasive. Applicant argues that Hirakata does not teach that the polarities are independently controlled for each vertical line. Examiner respectfully disagrees. Hirakata

provides means for controlling each vertical line's polarity individually (see FIGS. 5-8; col. 13, line 26 – col. 14, line 39). As to newly added claims 40-47, the arguments are moot in view of presented above grounds of rejection.

Conclusion

6. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

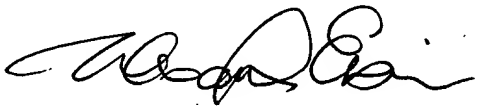
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (703) 306-2988. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (703) 308-6725. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 31, 2005



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